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Quasi Z-Source Converter Fed Inverter with Active Switched Network

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Abstract: This paper presents a quasi-Z source converter fed inverter with active switched networks. The converter topology is implemented with the help of capacitor, inductor and diodes connected in such a manner to improve voltage gain. A novel active switching network is developed to improve the harmonic performance of converter. Thus, network designed uses a combination of active switches and diodes to reduce the voltage and current ripple in the quasi-Z source converter. The performance of proposed converter is evaluated using a simulation. The results proves that the proposed converter can achieve a better harmonic performance than a conventional converter.

Key Word: voltage gain; Switched network; quasi z-source converter.

1. Introduction

For smooth functioning in electric vehicles, industrial drives, and other applications using varying frequencies need inverters. Two-level voltage source inverters typically meet the inverter requirement for these uses (VSI). VSI has a number of short comings.1) Buck surgery is a only option.2) Dead time must be allowed for the secure commutation of the semiconductor switches. 3) EMI is an issue. Cascading a boost converter with an inverter can help with the first issue. Two significant issues, however, are further compounded by this solution:1)Two-stage power conversion reduces effectiveness. 2) The life of the battery is short due to the EMI issue.

A new class of inverters called Z-sources inverters is developed to address these issues. The characteristics of both VSI and CSI are incorporated into Z-source inverters. The Z-source inverter offers enhanced capacitor lifetime, EMI immunity, dead-timeless operation, and Buck-Boost feature in one stage. A few disadvantages of the conventional Z-source network include uneven capacitor deterioration, high startup current, and discontinuous input current. Unusual incoming current results in high current load on the source. Occasionally, the uneven deterioration of capacitors and high startup current can damage semiconductor switches and lead to control problems. The number of passive components is also greater in Z-source inverter.

Several stated modifications are meant to address Z-source inverter issues. To lessen the use of passive components, the quasi-switched boost inverter is developed. However, increase in voltage is restricted.

To boost voltage gain, a novel switched inductor network-based Z-source converter fed inverter was developed. However, efficiency and input current are severely reduced with a greater element count, as well. In contrast to Z-source inverter, a quasi-Z-source converter can integrate switched inductor network to boost the input current. There are a number of other ZSI/qZSI networks that have been reported, such as switched Z-networks and diode assisted networks, which have greater voltage gain and lower voltage stress than conventional ZSI/qZSI networks. For high gain, however, is attained at the expense of greater number of components, so in reality, the cost and size are raised. Comparatively speaking, coupled inductor-based Z-source converters have a greater chance than these topologies.

A switched inductor (qZSI) capacitor with active switches is found to be a possible remedy. Since fewer passive elements are needed, the voltage stress on switching components is reduced while still providing greater boosting. This topology's regarding multi-cell network is suggested in the same article. Two multi-cell and switched capacitor/active switched inductor schemes that aim to further increase voltage gain are described. Promising voltage gain and better harmonic performance is offered by the described topologies. The voltage gain, however, can be increased while maintaining the same element count, provided that the voltage stress is decreased and the input current is maintained as

continuous.

In short, are volutionary high voltage gain converter addresses the demand for high voltage gain. There commended inverter consists of switched inductor and a capacitor network. The characteristics of recommended converter includes improved voltage gain, continuous input current and reduced voltage stress. A full evaluation of the suggested inverter's performance in contrast to the present topologies is also offered. The experiment serves as proof that the suggested converter functions.

2. Materials and Methods

A. Proposed Design

Proposed architecture seeks to provide maximum voltage gain with the least elements. The quasi-switched boost design is where the proposed topology draws its inspiration (qSBI). For a greater voltage gain, the qSBI is extended and changed. As shown in Figure (I), the suggested topology also includes qSBI, a diode, a inductor network and capacitors. It provides a continuous input current because the inductor has series connection with DC source.

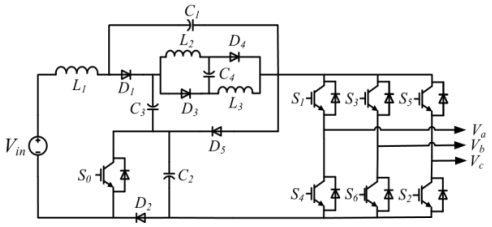


Figure (I)- Proposed Topology

B. Operation

The two states operations are distinguished in the proposed topology, and each is discussed in the next section

1) Shoot through State: Switch S0 is ON when in shoot-through mode. The switches on two of the inverter's legs are also switched ON at the same time. The inductor L1 is billed the amount during this time of voltage *Vin + VC1+VC2*. Reverse bias is present in diode D1 due to voltage's polarity across inductor L1. Due to the voltage on the capacitor C2, the diodes D2 and D5 are also reverse biased. The diodes D2 and D3 are forward-biased. The difference between the capacitors C3 and C4 charges the inductors L2 and L3.KVL is used to arrive at the following equation, Figure (II).

$$VL1=Vin+VC1+VC2 \quad (1)$$

$$VC2-VC3=VC4=VL2=VL3.(2)$$

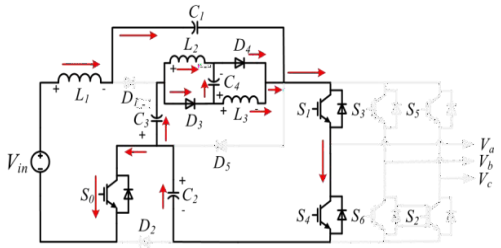


Figure (II)-Shoot _through State

2) Non-Shoot through State: Switch S0 is turned off when the device is not in a shoot-through state, operating the inverter either in active or zero states. When input voltage increases, the inductor L1 begins to discharge its energy into the load. The diode D1 is in a forward biased state as a result of the inductor L1'spolarity changing during discharge. D2 and D5 are also forward biased diodes. Because of the polarity of the inductors L2, L3, the diodes D3and D4 are reverse biased. The voltage across converter in this condition is that of the capacitor C2. According to Figure(III), the comparable circuit for this state. The subsequent equations can be found using KVL:

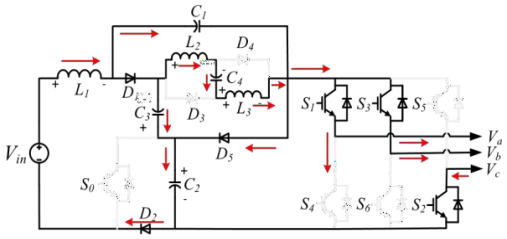


Figure (III)-Non shoot_through State

$$V_{L1}=Vin+V_{C3}-V_{C2}\,(3)$$

$$V_{L2}=\frac{VC4-VC1}{2}\,(4)$$

$$V_{C1}=V_{C3}\,(5)$$

$$V_0=V_{C2}\,(6)$$

C. Steady State Analysis

1).Voltage Gain Calculation

All semiconductor devices are considered to be perfect in nature to derive voltage gain. We assume, there is zero internal resistance for all passive components.

By applying energy conservation over inductor L2:

$$\text{D}\,(V_{C2} - V_{C3}) + (1\text{-D})\frac{(VC4-VC1)}{2} = 0 \quad (7)$$

The voltage $VC2$ is given by

$$V_{C2} = \frac{2}{1+D} V_{C1} \quad (8)$$

By applying the energy conservation principle across $L1$,

$$D(Vin + V_{C1} + V_{C2}) + (1-D)(Vin + V_{C3} - V_{C2}) = 0 \quad (9)$$

Rearranging above equation,

$$V_{in} + V_{C1} - (1-2D)V_{C2} = 0 \quad (10)$$

Substituting V_{C2}, V_{C1}becomes,

$$V_{C1} = \frac{(1+D)}{1-5D} Vin \quad (11)$$

Hence, voltage V_{C2} is given as

$$V_{C2} = \frac{2}{1-5D} Vin \quad (12)$$

The voltage V_{C4} is calculated as

$$V_{C4} = \frac{1-D}{1-5D} Vin \quad (13)$$

Final voltage gain at DC link is given by

$$\frac{V0}{Vin} = \frac{2}{1-5D} = B \quad (14)$$

where B= boost factor for inverter.

For 3-Ø inverter, peak AC voltage to input voltage ratio is given by $\frac{Vac}{Vin} = \frac{MB}{2}$.

On subs the DC gain value, the 3-Ø AC gain is given as

$$\frac{Vac}{Vin} = \frac{M}{1-5D} = G \quad (15)$$

where M= modulation index

2). Inductance Calculation (at Boundary of CCM)

According to power balance theory and ideality of inverter components, the eqn is given by

$$VinIin = V_0 I_0 \quad (16)$$

from Figure.2, Figure.3, input current = inductor current $L1$.Hence, average inductor current in $L1$=average input current, i.e.,$IL1 = Iin$.

From Equation-(16), average inductor $IL1$ is given by

$$I_{L1} = \frac{2}{1-5D} Vin \quad (17)$$

According to charge principle, average current in inductor $L2$ is calculated in capacitor $C3$. By applying charge balance theory, the ON and OFF current period in capacitor $C3$ is given by

$$i_{C3on} = 2i_{L2} + \frac{1-D}{D} i_{L1}, \; i_{C3off} = \frac{D}{1-D} i_{L1} - i_{L2} \quad (18)$$

Using charge balance theory,

$$\text{D}\,i_{C3on} = (1\text{-D})\; iC3off \quad (19)$$

By adding eqn (17),(18),(19),the average inductor current L2 is

$$I_{L2} = \frac{1}{1-5\text{D}} \text{Io} \quad (20)$$

From eqn (1), voltage eqn for inductor L1 is given by

$$\text{L1}\frac{\Delta iL1}{DTs} = \frac{4-4D}{1-5D} Vin \quad (21)$$

At boundary of CCM,$I_{l1} = 2\, I_{L1}$ the inductance L1 is determined by

$$\text{L1} = \frac{D(1-D)Vin}{Iofs} \quad (22)$$

wherefs=switching frequency

from equation (2), voltage eqn for inductor L2 is

$$L2\,\frac{\Delta iL2}{DTs} = \frac{1-D}{1-5D} Vin \quad (23)$$

Similarly,at boundary of CCM$i_{L2} = 2I_{L2}$,hence the inductance L2 is

$$L2 = \frac{D(1-D)Vin}{2I0fs} (24)$$

3. Result

The proposed converter fed inverter in this case is validated by MATLAB/Simu link simulation. For experimental validation, a prototype that resembles Fig is developed. The parameters for the suggested inverter are L1= 1000 µH and L2=500µH and C1=C2=C3=100µf,fs=10kHz,Rper phase=100ohms, Vin=40V. The inverter design is at modulation index M =0.85 and duty cycle D = 0.13 to gain the rms line –line voltage which equals to110V.

The DC link voltage at this operating pointis 5.4 times larger than the input voltage seen in Figure (V). None the less, the experiment's DC link voltage is 5.2 times the input voltage, was 208V at 40V.The actual voltage is thus less than the predicted voltage as a result of parasitic in passive and active components, as seen in figure. Furthermore, voltage spikes have been observed experimentally in the DC link voltage as a result of the formation of Nz-Dcm at a few locations. Yet,it is absent from simulation because of its ideal character, as seen in Figure. The current profile in inductors exhibits a positive and negative slope during ST and nST in both simulation and experiment, respectively.

The average current of inductor L2 is 2A as opposed to the simulation's result of 4.1A. which is somewhat higher, due to the existence of parasitic .The voltage of capacitor is also shown experimentally in Figure (IV) and (V). For the capacitors C1,C2 and C3 respective voltages of 110V, 208V and 82V are applied. The obtained DC link voltage is shown in Fig. to have a maximum output AC voltage per phase of 91.8 V for simulation and experiment, respectively, and 90 V at a modulation index of 0.85. As a result, the line-to-line voltage has an approximate rms value of 110 V in both simulation and experiment. Using data points, the total harmonic distortion (THD) is examined. 1.36% THD is detected for the voltage.

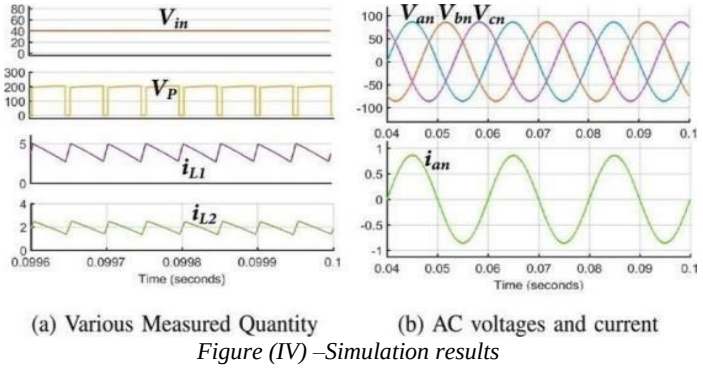


Figure (IV) –Simulation results

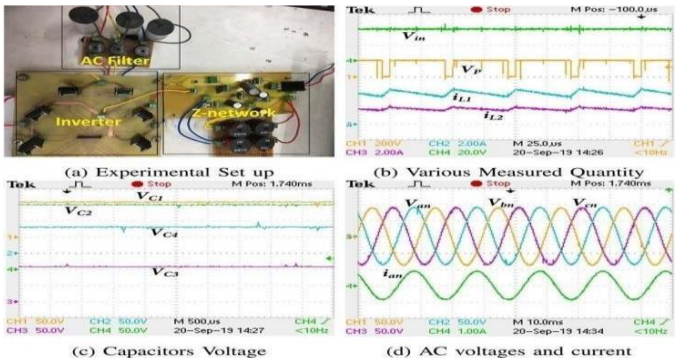


Figure (V)- Experimental results

4. Discussion

The Z source inverter's strong voltage gain at higher modulation indices plays a key role in enhancing the voltage quality. It's interesting that a greater modulation index can improve the suggested inverter's voltage gain. Several contemporary topologies are taken into account in order to compare the feature of the suggested inverter. Those topologies and their component counts is displayed in Table. Ip/Il ratios are all displayed in TableI.

A. Boost Factor

In Table1,Provides the duty cycle D and input voltage Vin are the same for all inverters, and shows that the suggested inverter has a larger gain than the topologies that are already in use. Moreover, Figure.VI-a displays the boost factor of the converter fed inverters. All inverters may, without a doubt, attain infinite gain with duty cycle modification. However, because the inverters contain parasitic organisms, they are subject to restrictions.

B. Voltage Stress

To achieve a similar voltage gain while lowering the voltage stress across inverter switches, suggested inverter uses a higher modulating index and a lower duty cycle. According to Fig, there is a voltage stress across the inverter. The suggested system delivers the lowest per unit stress when compared to the majority of current topologies, particularly HmcaSL/Sc-QZsi. To prepare for the worse, itis a good idea to have a backup strategy. The cost of there commended

inverter is cheaper than that of Hmc ASI/SC-QZsi and McASc-QZsi because it places less voltage stress on capacitor.

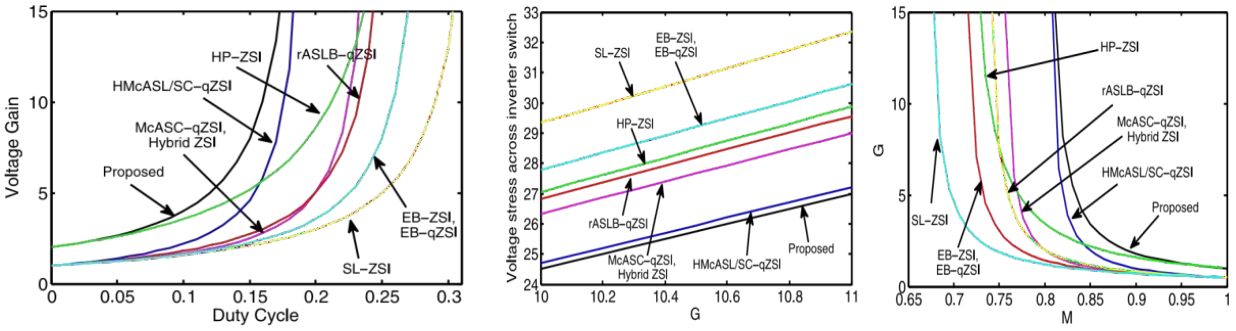
C. Output Voltage Quality

When considering THD, the output voltage quality is crucial. Better THD profiles for the inverter is realized at higher modulation indices. As shown in figure (VI), the proposed inverter is superior to all other topologies in that it can achieve a comparable. The essential requirement for all of these sources is that the inverter should have a zero-ripple current or continuous input voltage gain at a high modulation index. Therefore, using the proposed inverter would result in lower THD. The source can typically be a battery, fuel cell, or solar power for high gain inverters current.

Table 1

COMPARISON OF PROPOSED TOPOLOGY WITH EXISTING TOPOLOGIES

Topology	*L*	*C*	*S*	*D*	TC	*B*	V_c/V_{in}	V_D/V_{in}	V_S/V_{in}	G	I_L/I_P	I_P	ΔI_{in}
Proposed One	3	4	7	5	19	$\frac{2}{1-5D}$	$\frac{1+D}{2}B, B$ $\frac{1-D}{2}B$	$B, B/2$	B	$\frac{M}{5M-4}$	$(1-D)B$ $\frac{1-D}{2}B$	$\frac{(1-D)V_P}{R_l}$	ΔI_{L1}
HMcASL/SC-qZSI [12]	2	2	8	7	19	$\frac{1+D}{1-5D}$	B	B	B	$\frac{(2-M)M}{2(5M-4)}$	$\frac{1-D}{1+D}B$	$\frac{(1-D)V_P}{R_l}$	$(1-D)I_L$
McASC-qZSI [12]	1	3	9	6	19	$\frac{1}{1-4D}$	B	B	B	$\frac{M}{2(4M-3)}$	$(1-D)B$	$\frac{(1-D)V_P}{R_l}$	ΔI_{L1}
HP-ZSI [13]	4	3	6	6	19	$\frac{2(1+D)}{1-4D+D^2}$	$B, B/2$ $\frac{1-D}{1+D}B, \frac{D}{1+D}B$	$B, B/2$ $\frac{1-D}{1+D}B, \frac{D}{1+D}B$	NA	$\frac{M(2-M)}{2M^2-1}$	$\frac{1-D}{1+D}B$	$\frac{(1-D)V_P}{R_l}$	$(1-D)I_L$
EB-ZSI [9]	4	4	5	6	19	$\frac{1}{1-4D+2D^2}$	$(1-D)^2B$ $(1-D)B$	B, DB $(1-D)B$	NA	$\frac{M}{2(2M^2-1)}$	$(1-D)B$ $(1-D)^2B$	$\frac{(1-D)V_P}{R_l}$	$(1-2D)I_{L3}-$ $-(1-D)I_P$
EB-qZSI [14]	4	4	5	6	19	$\frac{1}{1-4D+2D^2}$	$(1-D)^2B, D(1-D)B$ $D(2-D)B$ $(1-3D+D^2)B$	B $3DB$ $(1-3D)B$	NA	$\frac{M}{2(2M^2-1)}$	$(1-D)B$ $(1-D)^2B$	$\frac{(1-D)V_P}{R_l}$	ΔI_{L1}
rASLB-qZSI [15]	3	3	6	7	19	$\frac{1+D}{1-4D+D^2}$	$DB, (1-D)B$ $DB, (1-D)B$	$B, (1-D)B$ $D\frac{2-D}{1+D}B, \frac{2-3D+D^2}{1+D}B$	NA	$\frac{M(2-M)}{2(M^2+2M-2)}$	$(1-D)B$ $(1-D)^2B$	$\frac{(1-D)V_P}{R_l}$	$\frac{D(1-D)B}{1+D}$
SL-ZSI [16]	4	2	7	6	19	$\frac{1+D}{1-3D}$	$\frac{1-D}{1+D}B$	$B, \frac{1-D}{1+D}B$ $\frac{D}{1-D}B$	NA	$\frac{M(2-M)}{2(3M-2)}$	$\frac{1-D}{1+D}B$	$\frac{(1-D)V_P}{R_l}$	$(1-2D)I_L - I_P$
Hybrid ZSI [17]	4	6	3	6	19	$\frac{1}{1-4D}$	$B, DB, (1-2D)B$ $2DB, (1-3D)B$	B	NA	$\frac{M}{2(4M-3)}$	$(1-D)B$	$\frac{(1-D)V_P}{R_l}$	ΔI_{L1}



(a) Boost factor comparison (b) Voltage across inverter switch (c) Overall Gain vs Modulation index

Figure (VI) -Comparative Analysis Graph

5. Conclusion

This article proposes a novel, high gain Z-source converter fed inverter. Among its contemporaries with a comparable component count, the suggested inverter has the largest gain. As a result, the DC link voltage is lowered in order to produce an AC gain that is comparable to that of other compared topologies. Also, voltage is reduced across inverter switches. The suggested inverter's constant input current lessens the source's exposure to current stress. Also, the suggested converter fed inverter run satD=0.13 and M= 0.85 in order provide 110 Vrms AC volt at 40 Vinput. Due to different voltage drops, the modeling results indicated a somewhat greater voltage than the results from the experiment.

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