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Multiphase Interleaved Converter Based on Cascaded Non-Inverting Buck-Boost Converter

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Abstract: This paper proposes an interleaved buck-boost converter with fewer switches. A single buck converter is followed by n parallel interleaved boost converters in the proposed converter. Aside from the reduced switch count, the proposed converter has the following benefits: soft start-up and shutdown capabilities. Furthermore, the buck stage protects power electronic devices and isolates the supply during load failure or overload. Furthermore, with the same switching scheme, the proposed converter can function as an interleaved boost converter for high voltage gain requirements. Furthermore, it provides quick dynamic performance with a smooth transition from buck to boost mode. This paper investigates the proposed three-phase interleaved buck-boost converter's eight operating zones for non-overlapping gate signal operation.

Key Word: Interleaved buck-boost converter; DC-DC converter; DCM (Discontinuous Conduction Mode)

1. Introduction

Electric cars, uninterruptible power supplies, micro grids, and renewable energy sources are just a few of the applications where dc-dc power electronics converters are employed extensively. The buck-boost converter may change the magnitude of the input voltage using a straightforward circuit and control loops through. With inverted output voltage, nevertheless, it has a constrained voltage gain. The buck-boost converter's operation in discontinuous conduction mode was suggested as a way to maximise voltage gain (DCM). Yet, because of greater current stress on power electronics devices, operation under DCM results in smaller converter passive parts and better dynamic performance. Presents two distinct topologies for lowering the present level of stress. In the first topology, two buck-boost converter inductors are charged in series and linked in parallel when being discharged, in contrast to the second topology, where the inductors are connected in parallel while being charged and discharged. The current stress on power electronics devices was reduced to half by the second topology, it was determined. When two or more converters are connected in parallel to create interleaving converters, the output voltage and rated output power of the converters can both be raised. When using a two-phase interleaved converter, the ripple frequency is twice as high as the switching frequency. A common inductor and an interphase transformer are used to double the ripple frequency in order to boost power density. The advantages of the cascaded noninverting buck-boost converter (CNIBBC) include lessened voltage stress and non-inverted output voltage polarity. Three CNIBBC are connected in parallel in and were running on DCM. The gate signals of each CNIBBC were not phase-shifted, hence the three converters are not functioning in an interleaved fashion. The boost units' blocking diode, which carries all of the discharging current, consequently inherits significant current stress. The grid-connected inverter's PV input voltage is increased by connecting two interleaved CNIBBC in parallel. The voltage stress on the power electronics switches is split between the boost switches, which experience the load voltage stress, and the buck switches, which experience the supply voltage stress, in the CNIBBC topology. The interleaved converter that is being proposed has a straightforward design, makes it simple to change the number of phases and allows for odd or even number of phases.

2. Methodology and Operations

The proposed three-phase interleaved buck boost converter is shown in Fig. 1. It is made up of a single buck converter (S0 and D0) and three parallelly connected boost converters that are interleaved (L1 to L3, S1 to S3, and D1 to D3). Three phase boost converter switches (S1 to S3) have the same duty cycle, but each gate signal is offset by 120

degrees from the one before it, as illustrated in Fig. 2. S0 is activated simultaneously with any of S1 to S3. As a result, the buck converter switch S0 gate signal is obtained via an OR logicgate with input signals S1 to S3. As a result, the buck *converter's* switching frequency is three times that of the boost converters. If the modulation index is greater than 1/n, the proposed buck switch is continuously activated, and the proposed interleaved converter operates as a conventional interleaved boost converter with no changes to the control loop or switching pattern. Because of this feature, the converter has a high voltage gain with a constant input current. Furthermore, the single buck switch extends the proposed interleaved topology's soft startup and shutdown capabilities.

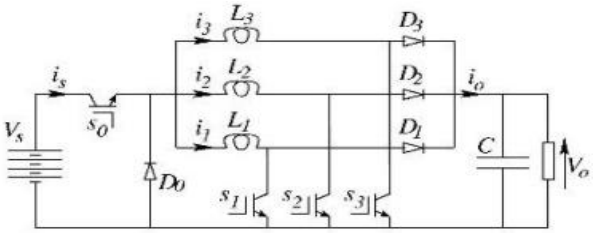


Fig 1. The interleaved converter circuit diagram

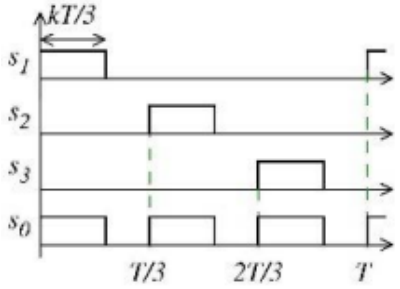


Fig 2. Switching signals

The duty cycle k must be less than 1/3 to operate non-overlapping gate signals, as shown in Fig. 1. (b). S0 becomes continuously conducting if the duty cycle exceeds 1/3, and the proposed converter operates as an interleaved boost converter. This action is appropriate for requiring a high dc-voltage gain. As a result, the proposed interleaved buck-boost converter has soft start and soft shutdown capabilities. As a result, the proposed interleaved buck-boost converter outperforms the conventional interleaved boost converter in performance.

Operations

For the proposed interleaved converter, there are numerous operational zones. The operation of non-overlapping gate signals is discussed in this paper. The inductances of the phase inductors are assumed to be the same. Fig. 3 depicts the eight zones of operation for a three-phase interleaved buck-boost converter that are determined by converter parameters such as inductance (L), switching frequency (f), duty ratio (k), and load resistance (R), where x = R/Lf. The subsections that follow present the gain equation and the boundary equations with the other zones for each operating zone. Winding resistances are ignored, and switches are assumed to be perfect. Because each inductor is only energised for one-third of the switching period, these assumptions are accepted for non-overlapping gating signal operation.

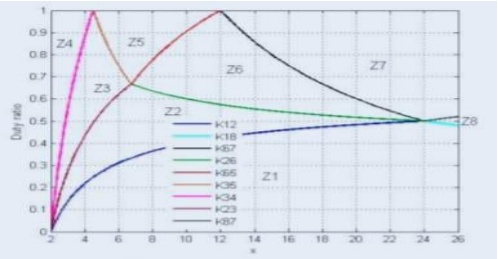


Fig 3. Interleaved converter operation

Zone 1

Figures 3(i) and 3(ii) depict the on-mode and off-mode circuits for zones 1, 2, 3, and 4. The current of the phase 1 inductor, i1, is traced in Fig. 3 for zone 1. (iii).The on-mode circuit's differential equations can be solved to obtain the peak currents, I1 and Ix, as follows:

$$I1 = kVs / 3fL \qquad (1)$$

$$Ix = k(Vs - Vo) / 3fL \qquad (2)$$

Where Vs and Vo are the supply and output voltages, and I1 is the DCM's global peak current. The proposed interleaved converter behaves as a buck converter during this zone because the inductors are always charging during on-mode. Because Ix is a positive number, this action can be deduced from (2). The intervals 1,1 and 2,1 are estimated from the off-mode circuit.

$$\delta 1,1 = k / 3fG1 \quad (3)$$

$$\delta 2,1 = K(1 - G1) / 3fG1 \quad (4)$$

The voltage gain of converter for zone1 is G1 = Vo / Vs

Using (1) and (2), the voltage gain of an on-mode circuit can be estimated

$$G1 = \frac{k^2 x}{6} \left(\sqrt{18 / k2\, x + 1} - 1\right) \quad (5)$$

If the current increases, 1,1 increases until it reaches (1k)/3f, at which point operation in Zone 2, Fig. 4(b), begins. The boundary condition in the k-x plane shown in Fig. 3, K12 is obtained by substituting (5) in (3) at 1,1 = (1 k) 3f as follows:

$$K12 = (4 - \sqrt{30\, x + 1})/5 \quad (6)$$

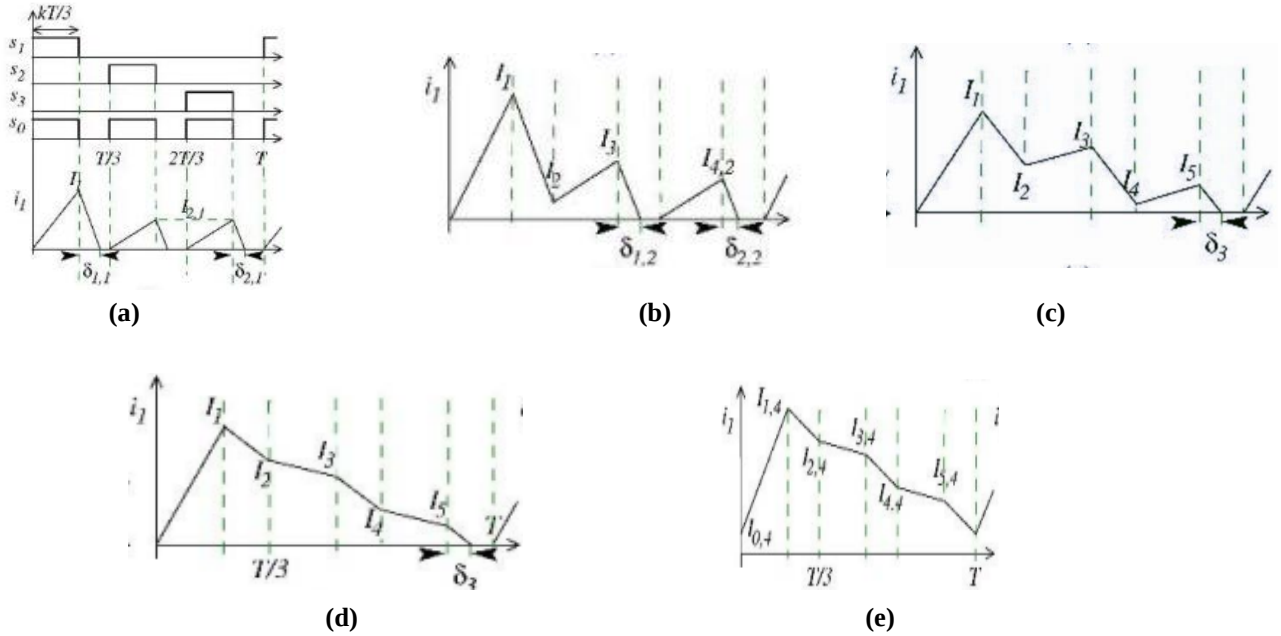


Fig 4. Coil current of phase 1 for : zone 1(a), zone 2(b), zone 3(c), buck, zone 3(d), boost, zone 4(e) of the proposed converter

Zone 2

Figure 3 depicts the zone 2 phase 1 inductor current waveform (b). The different peak currents and time intervals are calculated after solving the on-mode and off-mode circuits as follows:

$$I_2 = [2kVs - (1 - k)Vo] / 3fL \quad (7)$$

$$I_3 = [2kVs - Vo] / 3fL \quad (8)$$

$$I_{4,2} = k(Vs - Vo) / 3fL \quad (9)$$

$$\delta_{1,2} = (2k - G2) / 3fG2 \quad (10)$$

$$\delta_{2,2} = k(1 - G2) / 3fG2 \quad (11)$$

As shown in (9), the proposed converter operates in buck mode during zone 2.

The voltage gain is expressed using the on-mode circuit and calculating the average supply current using (1) and (7) to (9).

$$G_2 = \frac{kx}{6} \left(\sqrt{30/x + 1}\right) \quad (12)$$

If the current increases, 1,2 increases until it reaches (1- k)/3f, at which point operation in zone 3 begins, as shown in Figs. 3(c) and (d). The boundary between zones 2 and 3, K23, shown in Fig. 2, is derived under these conditions by substituting (12) in (10),

$$K_{23} = \frac{2}{5} \left(4 - \sqrt{\frac{(30}{x} + 1}\right) \quad (13)$$

Zone 3

Figures 3(c) and (d) show the phase 1 inductor current waveforms for zone 3 buck and boost operations, respectively.

The different peak currents and time intervals 1,3 are formulated as follows after analysing the on-mode and off-mode circuits:

$$I4 = [2kVs - (2 - k)Vo] / 3fL \quad (14)$$

$$I5 = [3kVs - 2Vo] / 3fL \quad (15)$$

$$\delta 3 = (3k - 2G3)\ 3fG3 \quad (16)$$

The voltage gain is,

$$G3 = kx / 6 \left(\sqrt{54/x + (3 - k)\ 2 - (3 - k)}\right) \quad (17)$$

Inspecting (17), the condition for buck operation, in zone 3, is given by the following inequality

$$k < 3 / 11 (1 + \sqrt{22 / 3x + 1}) \quad (18)$$

If the load is increased further, which is indicated by zone 4 in Fig. 3, Continuous Current Mode (CCM) is activated (e).

The boundary condition between zones 3 and 4, K34, can be obtained by substituting 1,3 = (1 k)/3f in the equation (16)

$$K34 = 3 - \sqrt{18/x} \quad (19)$$

The minimum inductance result under CCM operation,

$$Lc = R / 18f (3 - k)^2 \quad (20)$$

Zone 4

This zone 4 represent the operation under CCM illustrated in Fig 3 (e). The peak current and voltage gain as follows:

$$I1,4 = Vo / R [1 / 3 - k + R / 3Lf (1 - k / 3)] \quad (21)$$

$$G4 = 3k / 3 - k \quad (22)$$

Zone 5

Figure 4 (a) shows the inductor current of phase 1. During off-mode, the slope of the current waveform is negative. This action indicates Vs Vo, revealing the boost operation. The differential peak currents and time interval 5 can be calculated using the following formula:

$$\delta5 = [2kVs - (2 - k)V_o] / 3f (Vo - Vs) \quad (23)$$

The voltage gain is,

$$G5 = [\frac{1}{2} + (1 - k)(2 - k)\frac{x}{6}] + \sqrt{[1/2 + (1 - k)(2 - k)\ x/6]\ ^2} - \frac{kx}{6}\ (6 - 7k) \quad (24)$$

It can be noticed that if δ5 = k/3f,

$$K35 = 9/2x \quad (25)$$

Zone 6

It the factor x is increased due to increase in load resistance, the peak currents and the time interval δ6 are given by:

$$\delta6 = (2k - G6) / 3fG6 \quad (26)$$

The voltage gain is,

$$G6 = \frac{kx}{12} (\sqrt{\frac{96}{x} + (2 - k)^2 - (2 - k)}) \quad (27)$$

When the current is increased until 6 = (1-k)/3f, zone 5 operation begins, and the boundary condition between zones 5 and 6, K56, is formulated by substituting (27) in (26),

$$K56 = 2(1 - \sqrt{3/x}) \quad (28)$$

The boundary condition K26 can be calculated by nulling (9), I4,2 = 0.

$$K26\ (1 + \sqrt{\frac{30}{x} + 1})/5 \quad (29)$$

(a) (b)

Fig 5. Phase1, coil current for zone 5 and zone 6

Zone 7

If the factor x is increased further, the proposed converter's operation is moved from zone 6 to zone 7.During the off-mode, the slope of the current waveform is negative, indicating boost operation. The following is how the peak currents and time interval 7 are calculated:

$$\delta7 = \frac{[kVs - (1 - k)Vo]}{3f (Vo - Vs)} \quad (30)$$

The voltage gain is as follows,

$$G7 = \left[\frac{1}{2} + (1 - k)^2 \frac{x}{12}\right] + \sqrt{[\frac{1}{2} + (1 - k)^2 \frac{x}{12}]^2 - \frac{kx}{6} (2 - 3k)} \quad (31)$$

If δ_7 = k/3f, zone 6 operation is started, and the boundary condition between zones 6 and 7, K67, is obtained by solving (30) and (31),

$$K_{67} = 12/x \quad (32)$$

Zone 8

Zone 8 is the final zone for the proposed interleaved converter's non-overlapping gate signals operation. Transfer from zone 7 to zone 8 at light loads. Boost operation continues in zone 8, as it does in zones 4, 5, 6, and 7. The time interval 8 is calculated as follows:

$$\delta 8 = \frac{k}{3fG8} \quad (33)$$

The voltage gain obtained is,

$$G8 = k\sqrt{\frac{x}{6}} \quad (34)$$

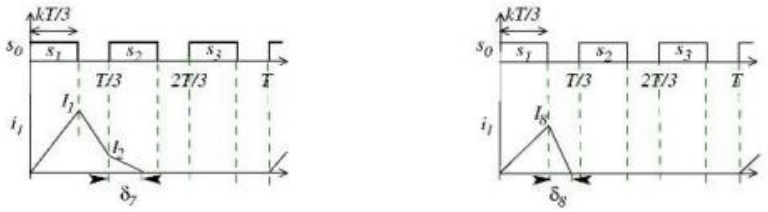
If δ_8 = (1 k)/3f, then the operation is in zone 7. The boundary condition between zones 7 and 8, K_{78}, is obtained by substituting (34) in (33)

$$K78 = 1 - \sqrt{\frac{6}{x}} \quad (35)$$

Finally, the boundary condition K18 can be calculated by equating the voltage gain of zone 1 (buck) or zone 8 (boost) to unity,

$$K18 = \sqrt{\frac{6}{x}} \quad (36)$$

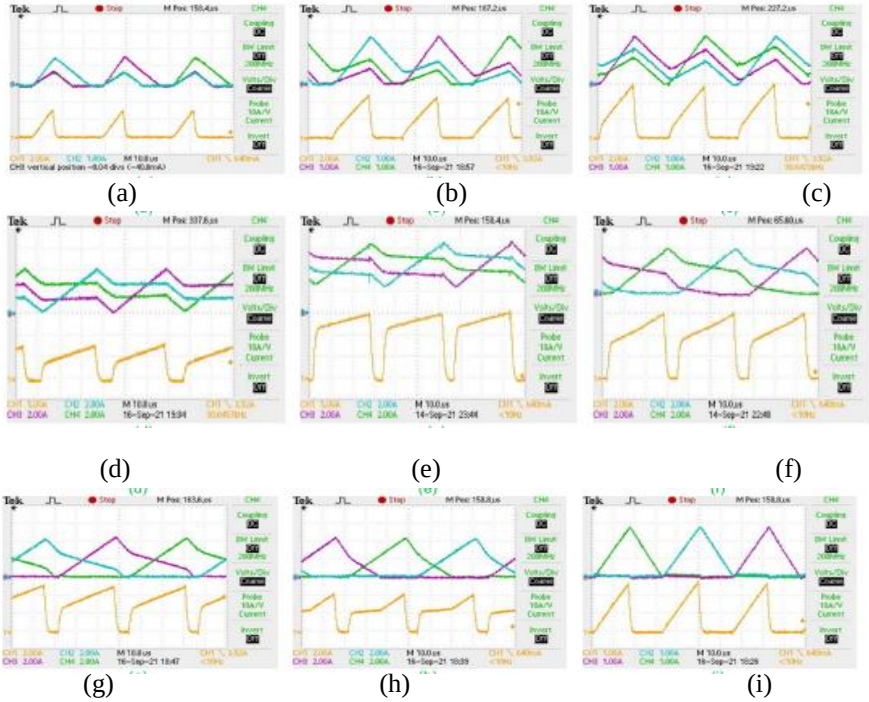
$x \rightarrow \infty$ at no load. K78 = 1 and K18 = 0, according to (35) and (36), respectively. When a light load is connected, this action reveals that the proposed interleaved converter operates at zone 8.



(a) **(b)**

Fig 6. Phase 1, coil current for zone 7 and zone 8

3. Result



(a) (b) (c)

(d) (e) (f)

(g) (h) (i)

Fig 7. (a) zone 1, (b) zone 2, (c) buck operation of zone 3, (d) boost operation of zone 3 , (e) zone 4, (f) zone 5, (g) zone 6, (h) zone 7, (i) zone 8 of proposed interleaved converter.

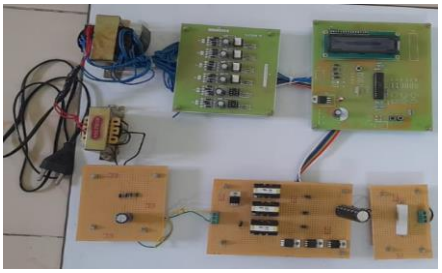


Fig 8. The Hardware setup of proposed converter

Figure 7 shows the currents of the buck switch and three phase coils during operation in different zones of the proposed interleaved converter. The eight operational zones discussed in and recognised. For zone 3, the buck operation is shown in Fig. 7(c), while the unity gain operation is shown in Fig. 7(d), where the duty ratio is set according to (18). The internal coil resistance per phase is responsible for the negligible differences between theoretical and experimental values. As expected, the effect of internal coil resistance on voltage gain can be ignored for non-overlap gate signal operation of the proposed interleaved converter. The figure 8 shows the hardware implementation of proposed converter. Here, we use microcontroller for programming, driver circuit is used for modify the signals which comes from microcontroller. These signals will pass to the MOSFET .Here we use DC source for input and we use DC-DC converter which consist of inductor- 1mH, high frequency diode, capacitor,mosfet-IRF840.

4. Discussion

DC-DC Converter performance

The proposed interleaved converter demonstrate the soft start-up. These proposed converter increase the output voltage. The result demonstrates one of the proposed converter's features, which is its operation as an interleaved boost-converter for high voltage gain. To demonstrate the proposed converter's behaviour under overload or load failure, the output current and voltage are suddenly changed from 100 to 10. It can be seen that the current limiter successfully limits the converter output current to its rated value, 2.5A, and protects the converter from damage

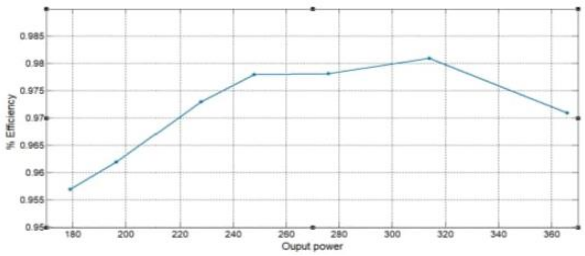


Fig 9. Efficiency of proposed DC-DC converter

The above figure shows the efficiency of the proposed DC-DC converter at different otput. The proposed converter has a high operating efficiency, as can be seen.

5. Conclusion

This paper describes an interleaved buck boost topology with a reduced switch count for dc-dc and ac-dc conversion systems. The buck stage provides numerous advantages for the proposed converter, including soft start-up without inrush current even during overload or load failure conditions. The characteristics of the proposed buck-boost interleaved converter during non-overlapping gate signals operation are investigated in this paper. The proposed converter has been found to operate in boost mode in five zones, buck mode in two zones, and buck-boost mode in one zone, Z3. The voltage gain and peak current are calculated for each zone and plotted against duty cycle, converter parameters, and load resistance. An experimental prototype is developed to verify the analysis and capabilities of the proposed interleaved buck boost converter.

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