INTERNATIONAL JOURNAL OF
RECENT TRENDS IN MULTIDISCIPLINARY RESEARCH
September-October 2021, Vol. 1(02), 11-13.

Implementation of Low-Power1-Bit Hybrid Full adder with Reduced Area

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Article Type: Research

OPENACCESS

Article CitationG.Arun Kumar1, J. Lokesh2, K. Sudhanshan3, Implementation of Low-Power 1-Bit Hybrid Full adder with Reduced Area, International Journal Of Recent Trends In Multidisciplinary Research, April 2021, Vol. 1(02), 11-13.

Receiveddate: September20,2021

Accepteddate: October05,2021

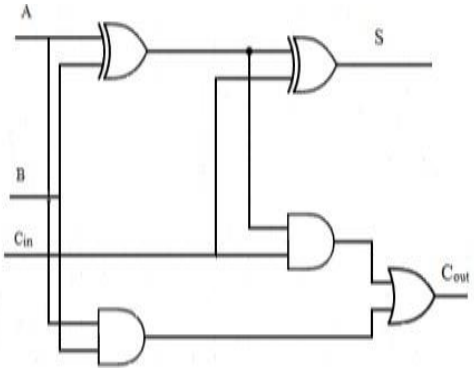
Published date : October12,2021

Abstract: In this investigation a low power 1-bithy bridfull snake (FA) and 4-digit full snake circuits where arranged with the proposed 1-bit full adder.By utilizing CMO Sand Pass transistor reasonings another XNOR reasoning is executed. The voltage degradation issue can be over powered by using the CMOS weak inverters.By using this power consumption can be improved.By utilizing two transistors,carry logic module is designed. The circuit is worked at 1.8v. The circuit is designed using 125nm advancement and cow hide treater EDA gadget is used to perform the reenactments. For the proposed plan of full adder the power consumed is of 763.5nW and the delay is 41.03ps.

Index Terms Area, Fulladder, Power, Tanner EDA software, XNOR.

1.Introduction

The movements in the VLSI development and the demand for the low power, less delay and growing the operating speed of the device[3].The main goals in VLSI is minimizing the semiconductor count,increasing the speed and minimizing the power usage. Number shuffling operations(Addition, Duplication, etc) are used in an extensive part of the VLSI applications. In basically everything estimations full snake is used. Theadder is a boss among the most fundamental bits of a process or that is included in the building block of Arithmetic reasoning unit [9]. Generally plans of adders are divided into two reasoning styles, static and dynamic reasoning styles[2].The reasoning style is chosen based on the requirement.Requirement of less power makes the static full adders simple,and reliable.The main problem in static full adders is area required is more when diverged from dynamic full adder[10]. As of now in special full snake, there are some advantages compared to the static reasoning styles, like fast trading speed,full swing at yield, etc. Combination full adders are utilized in the battery-worked minimal devices,for example,mobile telephones,PDA's,and notepads which require in VLSI, and Ultra Colossal Degree Facilitated circuits (ULSI) plans with a superior power postpone angles [8].It is utilized in the Processor chip like Intel Pentium for CPU part,which comprises ofALU.This is used to do the tasks like derivation, and so on [4]. In this research 1-digit full snake design is proposed using revised carry reasoning module and XNOR module, that consumes very less power than that of the flow circuits. Use of XNOR in the full snake decline the power usage by introducing a weak inverters.



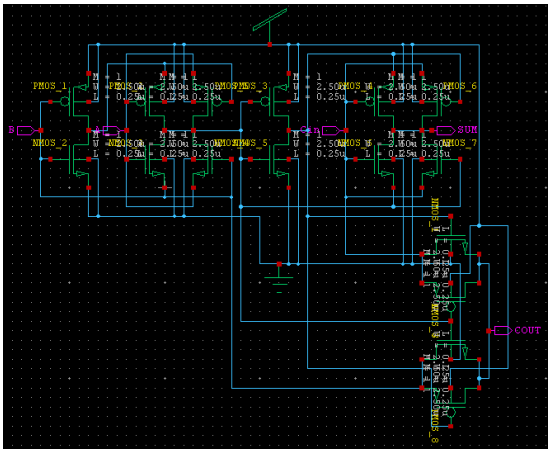


Fig.1 Full Adder circuit using logic gates.

XNOR Module:-

Fig.5 Modified Full Adder

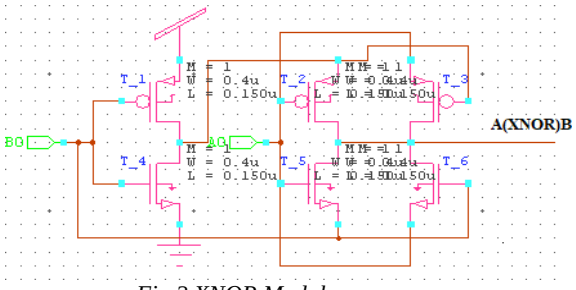


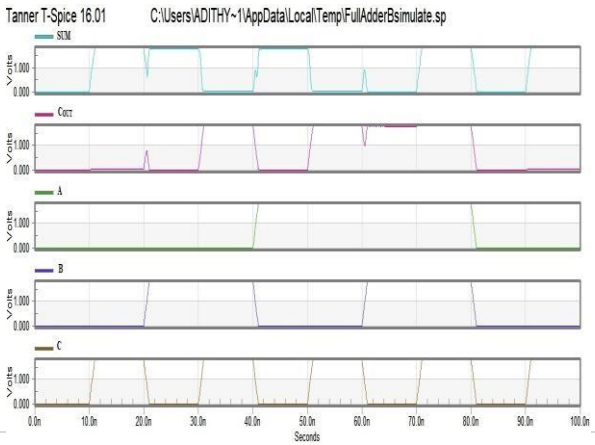
Fig.2 XNOR Module

By using XNOR module the power consumption is also dominated with introducing a Buffer which have small channel width, containing T_1 (Semiconductor 1 PMOS) andT_2 (Semiconductor 2 PMOS). Pad yield is used to outline a controlled inverter using T_3 (Semiconductor 3 PMOS) and T_4(Transistor 4 NMOS) semiconductor. However T_5 (Semiconductor 5NMOS) and T_6 (Semiconductor 6 NMOS) structure a level restorer that is at risk for going completely out of the outcome signal [5-6].XNOR module contains six semiconductors in a manner that,the power is consumed less[7].

1-Bit Full Adder:-

Snake is essential part in PCs. Equivalent augmentation is one of the basic task in PC number rearranging. Generally a1-bit full adder is an arithmetic operation used for adding(A,B, Cin) three commitments of a full snake. The outcomes are absolute and carry. The current (Fig.2) and proposed full snake (Fig.5)have two blocks. Beginning one is two XNOR modules that will produce the Aggregate and one Convey age module for instance for producing Cout.The existing full snake involves 16 transistorsin complete for instance 8-PMOS and 8-NMOS semiconductors. In proposed full adder1-PMOS and1-NMOS transistor is removed,resulting the total transistors count to 14.The 4-bit Full Adder is designed using 4 modified 1-bit full adders.

2..Result



TABLEIII Parameters of Proposed Full Adder

Transistor count	Area (μm^2)	Power (nw)	Delay (ps)
14	88.31	763.5	41.03

4-BitFullAdder:-

4 bit Full adder (FA) is an arithmetic (combinational) circuit that can be used to add 3 data pieces to produces um and carry yields. A, B, C in are inputs. The essential block for arranging the 4-digit full snake (FA) is 1-cycle full adder(FA).The modified 1-bit full adder(FA) block is utilized to execute design.C3 is the do of the circuit and sum(S0,S1,S2,S3).The first full adder(FA) **Cout** is given to these cond full adder (FA)Cin .The second full adder (FA)Cout is given to the third full snake (FA) Cin.The third full adder (FA) Cout is given to the fourth full adder(FA)Cin.Simulation results are performed in tanner tools.

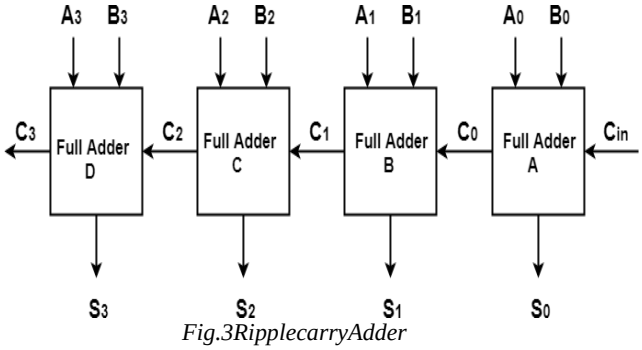


Fig.3RipplecarryAdder

3.Conclusion

A low power and high speed full adder circuit is designed and simulated in 125nm technology, by introducing modified Convey age and XNOR module into the circuit using Tanner EDA gadget. From the repeated yield it has been observed that the area of full adder circuit is reduced by 10%and the power consumed was seen as 763.5 nW which is less than the existing circuits and the delay is 41.03ps.

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